REMARKS

Claims 15 and 34-56 are allowed.

Claims 1-3 and 10 stand rejected.

Claims 4-9 and 11-14 are objected to.

Claims 57-66 are added. No new subject matter is present.

Claims 1-15 and 34-66 are pending.

Claim Rejections – 35 § 102

Claims 1-3, 10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,926,384 to Roy ('Roy'). The applicants disagree for the following reasons.

With regard to claim 1, it recites a read charge control circuit activated only during read operations by a read signal and an address. After reading the office action, it is somewhat unclear as to what specific structure found in Roy the Examiner considers to be the recited read charge control circuit. For this reason the applicants respectfully request the Examiner's patience in the following discussion.

For example, in column 7, lines 10-20, Roy actually describes how two local column decoders (that are not shown in the Figures) decode column address signals to ***generate*** column address signals CRD (emphasis added). The Examiner has already indicated that Roy's CRD signal corresponds to the recited read signal in claim 1 (Office Action, section 4). Consequently, it is apparent that the two local column decoders are not the recited read charge control circuit because ***they are not activated*** by the signal CRD, rather, ***they produce*** the signals CRD (emphasis added).

The question then becomes what exactly does Roy's CRD signal activate? Roy teaches that only one CRD signal is enabled during each memory access cycle (column 7, lines 15-16). The decoded column read signals (CRD) are used by the multiplexer 78 to couple one of eight memory columns 74 to a pair of common data out lines CDO-CDOLB 80-82 (FIG. 7; column 7, lines 1-5). Thus, it is apparent that the multiplexer 78 is not the recited read charge control circuit because it is only "activated" by the enabled column read signal CRD, and not by a read signal ***and*** an address as recited in claim 1.

Jumping ahead for a minute to claim 2, it recites that the read charge control circuit is a sense amplifier. The Examiner has stated that this limitation is disclosed by Roy in column 7, lines 30-34 (Office Action, section 4). If, then, the recited charge control circuit of claim 1 is disclosed by Roy's sense amplifier 64 of FIG. 7, the sense amplifier 64 must be analyzed to see if it meets all the requirements of claim 1. Roy's sense amplifier 64 is coupled to the pair

of common data lines CDO-CDOB (FIG. 7; column 7, lines 31-34). The two remaining inputs to the sense amplifier 64 are labeled SA and EQB, and it is apparent from Roy's description that these signals are, respectively, a pull-down signal and an internal equalization signal (column 12, lines 13-25). Consequently, Roy's sense amplifier 64 cannot be the recited read charge control circuit of claim 1 because it is not activated only during read operations by a read signal and an address as recited in claim 1.

Likewise, the combination of the multiplexers 78 and 78' and the sense amplifier 64 cannot be the recited read charge control circuit because in that case there would be three inputs (CRD, SA, and EQB) to the read charge control circuit, and claim 1 recites that the read charge control circuit is activated only during read operations by a read signal and an address.

Furthermore, claim 1 recites a write charge control circuit activated by a write charge signal and the same or different address. The Examiner has stated that Roy's WEP pulse generator and Roy's WBX signal anticipate the write charge control circuit and the write charge signal, respectively (FIG. 9; column 7, line 60 – column 8, line 20). However, Roy states that the WEP pulse generator 58 generates a downward pulse on either the WEPL or WEPR lines, depending on the value of the A8 address signal ***at the end of each write cycle*** column 7, lines 60-63; emphasis added). Consequently, the WEP pulse generator is not activated by the A8 address signal because the A8 address signal merely determines whether a pulse is generated on the WEPL or the WEPR line. In other words, the WEP pulse generator is activated regardless of the A8 address signal. As shown in FIG. 9, the WEP pulse generator 58 is ***inactive*** when the chip enable signal CEB is high (column 7, lines 64-66; emphasis added). The CEB signal is not the same address or a different address, as recited in claim 1. Additionally, because the value of the A8 address signal is only used by the WEP pulse generator at the end of each write cycle, this is yet a further indication that the A8 address signal does not activate the WEP pulse generator as is required by claim 1.

Claim 1 also recites that the read charge control circuit and the write charge control circuit are both coupled to a first and a second data IO line, wherein the secondary data IO line is complementary to the first data IO line. Roy also fails to disclose this limitation. If Roy's WEP pulse generator 58 is the write charge control circuit, then it is coupled to the WEPL and the WEPR lines (FIG. 9, column 7, lines 60-62). If Roy's sense amplifier 64 is the read charge control circuit, then it is coupled to the common data lines CDO-CDOB (FIG. 7; column 7, lines 31-34). It is apparent that the WEPL/WEPR lines are not the same as the CDO/CDOB lines.

Regarding claims 2, 3, and 10, the applicants submit that they are allowable for at least the same reasons as claim 1.

Allowable Subject Matter

Claims 15 and 34-36 are allowed.

Claims 4-9 and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In keeping with the Examiner's suggestion, new claims 57-66 are added. Independent claim 57 contains the limitations of claim 1 and 4. Claim 58 contains the limitations of claim 5 and is dependent upon claim 57. Claim 59 contains the limitations of claim 6 and is dependent upon claim 57. Independent claim 60 contains the limitations of claims 1 and 7. Claim 61 contains the limitations of claim 8 and is dependent upon claim 60. Claim 62 contains the limitations of claim 9 and is dependent upon claim 60. Independent claim 63 contains the limitations of claims 1, 10, and 11. Independent claim 64 contains the limitations of claims 1 and 12. Claim 65 contains the limitations of claim 13 and is dependent upon claim 64. Claim 66 contains the limitations of claim 14 and is dependent upon claim 65.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-15 and 34-66 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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